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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/061,152	02/04/2002	Shigeru Hasegawa	218008US-2 CONT	1853

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EXAMINER	
KANG, DONGHEE	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/061,152	HASEGAWA, SHIGERU	
	Examiner	Art Unit	
	Donghee Kang	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7,8 and 11-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7,8 and 11-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/314,115* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continuing Domestic Data

1. Acknowledgment is made that this application is a continuation of Application Serial No. 09/314,115, filed 19 May 1999, which is issued as U.S.Patent No.6,392,272.

Drawings

2. The drawings are objected to because numeral "5" in Fig.10 does not connect to the gate oxide layer which is formed inside the trench. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 7 is objected to because of the following informalities: in line 13, the phrase "twos" is misspelled. It should be - -two - -. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims **7-8, & 11-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuwahara (US 5,821,580).

Re Claims **7-8, 12 & 14**, Kuwahara teaches an insulating gate type semiconductor device comprising (Fig.8):

a semiconductor substrate on which a P-type emitter layer (10), an N-type base layer (11) and a P-type base layer (12) are formed in sequence from the underside thereof to the surface thereof; a plurality of trenches arranged substantially in parallel throughout said semiconductor substrate and each recessed at a first distance and a second distance alternately, lower ends of said trenches extending to a depth extending from the surface of said semiconductor substrate to an upper portion of said N-type base layer,

a gate oxide layer (15) provided on an inner surface of each of said trenches an don the surface of said semiconductor substrate;

a plurality of sets of trench gate electrodes (16) each provided in said each trench formed with said gate oxide layer, with one set of said trench gate electrodes being constituted by two arranged in sequence at the first distance and said first distance is greater than said second distance, wherein the first distance is longer than the second distance;

an N-type emitter layer (13) provided in the surface part of said P-type base layer having a length of said second distance interposed between said trench gate electrode belong to said one set of electrodes and said trench gate electrodes belonging to another set of electrodes adjacent to said one set of electrodes, and in the vicinity of said trench gate electrode;

an insulating oxide layer (31) provided covering a part or whole of said trench gate electrode, and holed with contact holes at each of portion provided with said P-type base layer and said –type emitter layer;

an emitter electrode (22 & 23) provided covering said insulating oxide layer and connected to said P-type base layer and said N-type emitter layer; and

a collector electrode (19) provided on said P-type emitter layer on the underside of said semiconductor substrate.

Kuwahara does not clearly teach a gate wire for transmitting a voltage applied to a gate. It is conventional in the art to form gate wiring in order to provide a voltage to the gate electrode. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the gate wiring in the device in order to provide a voltage to the gate electrode so as to operate the device.

Kuwahara does not expressly teach the predetermined depth of the trench is set to such an extend that a depletion layer formed extending from top of said trench gate electrode when in a forward voltage application is fused with a depletion layer formed extending from a junction area between said N-type base layer and said P-type base layer to which said trench gate electrode is vicinal and that a curvature of said depletion layer at the top of said trench gate electrode is relieved. This feature is inherent in Kuwahara's device because in Kuwahara's device lower ends of the trenches is extending to a depth extending from the surface of the semiconductor substrate to an upper of said n-type base layer.

Re Claims **11 & 13**, Kawahara does not expressly teach the predetermined depth of the trench is such a depth that a depth from the junction surface between said N-type base layer and said P-type base layer is 3 μm or less.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to select the depth of the trench, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 703-305-9147. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Donghee Kang
Examiner
Art Unit 2811

dhk
July 21, 2003